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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,523	03/12/2001	Michael T. Moore	0325.00361	9089
21363	7590	08/02/2004	EXAMINER	
CHRISTOPHER P. MAIORANA, P.C.			TRAN, ANH Q	
24840 HARPER			ART UNIT	PAPER NUMBER
ST. CLAIR SHORES, MI 48080			2819	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/804,523

Applicant(s)

MOORE, MICHAEL T.

Examiner

Anh Q. Tran

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-22 and 24 is/are rejected.
- 7) ☒ Claim(s) 4 and 23 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5, 7-22, 24 are rejected under 35 U.S.C. 102(e) as being anticipated by New et al (6,362,650).

Claim 1, New shows an apparatus comprising:

One or more logic circuits (100, Fig. 2) configured to provide logical operation, wherein the one or more logic circuits comprise programmable logic elements (CLB) and non-programmable hard wired blocks (303, Fig. 3, col. 3, lines 62-67) having no programmable elements within a programmable logic device, wherein the programmable logic elements are configurable between two or more different logical functions and connectable by a routable interconnect circuit (Switch, Fig. 2).

- Claim 2, New shows the one or more logic variable width logic circuits (302, Fig. 3).

- Claim 3, New shows a width each of the one or more logic circuits is determined in response to one or more input signals (col. 4, lines 1-5).

Claim 5, New shows one or more of the non-programmable hard wired blocks comprises a hard wired multiplier (402, Fig. 4).

Claim 7, New shows one or more of the logic circuits are configured to present one or more outputs (407a, 408a).

Claim 8, New shows the one or more outputs comprise intermediate signals (407b, 408b, 408c, 407c).

Claim 9, New shows an adder circuit (col. 3, line 66) configured to receive the one or more outputs (other 102 or adder circuit receive the one or more output signal through OMUX 601, col. 6, lines 64-67).

Claim 10, New shows the routable interconnect circuit is configured to route one or more of signals to one or more of the non-programmable hard wired blocks and signals from one or more of the non-programmable hard wired blocks (col. 3, lines 30-48).

Claim 11, New shows a number of registers (registers, col. 3, line 61) configured to increase a throughput of the one or more logic circuits.

Claim 12, New shows each of the one or more logic circuits comprise an input portion configured to store one or more input signals (latched, col. 5, lines 38-40).

Claim 13, New shows each of the one or more logic circuits comprises an output portion configured to store an output (inherent limitation since a dual-RAM have latched for outputting the signals).

The limitations of claim 15 is rejected as above.

The apparatus above is applicable to the method claims 16-20.

Claim 21, New shows the non-programmable hard wired blocks comprise dedicated logic having a fixed implementation of a given functional block on silicon.

Claim 22, New shows the programmable elements comprise configurable macrocells (col. 3, lines 3-29).

Claim 24, New shows the non-programmable hard wired block comprise hard wired multipliers having a first width and are couplable to form one or more multipliers having a second width (402, Fig. 4 are couplable together through 301, 304-306).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over New et al (6,362,650).

New discloses the claimed invention except for one or more of the non-programmable hard wired blocks are configured to perform cyclic redundancy check functions. It would have been an obvious matter of design choice to provide the non-programmable hard wired blocks configured to perform cyclic redundancy check functions, since New teaches that an alternative structure 303 may be any suitable dedicated circuit known in the art and selected by the FPGA architect (col. 3, lines 62-67).

Allowable Subject Matter

5. Claims 4 and 23 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

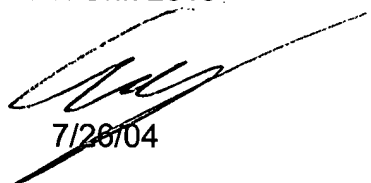
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh Q. Tran
Examiner
Art Unit 2819



7/26/04